# 53A-241 ARBITRARY WAVEFORM GENERATOR CARD

# OPERATING MANUAL



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# 53A-241 ARBITRARY WAVEFORM GENERATOR CARD

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## DESCRIPTION

The 53A-241 Arbitrary Waveform Generator (ARB) Card is a printed circuit board assembly for use in a CDS 53/63 Series System. The card produces a series of voltage samples to create precise sinusoidal, triangular, square, and user-defined arbitrary waveforms. The ARB Card produces an analog output of ±5.11 V in digital steps with 10-bit resolution (10 mV/step) when driving a 50-Ohm load, or ±10.22 V (20 mV/step) when driving a high-impedance load.

Eighteen different sample update rates are programmable, covering a 6.5-decade range from a high speed of 2 MHz to a low speed of 4 Hz. Up to 8,192 10-bit voltages may be programmed into the on-card memory. The memory may be partitioned into two 4K-word blocks or a single 8K-word block. When partitioned as two 4K blocks, one memory partition may be updated while the other is transmitting.

The waveform in each partition may be of any length up to 4,096 samples. Each waveform may be independently programmed to repeat from 1 through 99 times, or continuously. The two partitions may also be chained together, and the chained composite of the two waveforms may be programmed to repeat from 1 through 99 times, or continuously.

Breakpoints may be programmed in any nonconsecutive memory locations. A breakpoint will temporarily pause the waveforms until retriggered by software or until an external hardware TTL trigger.

Memory locations are easily programmed by a string of numeric ASCII characters which directly represent the voltage output for that sample. An editing capability is provided to allow changing of individual points in the waveform without requiring a complete reloading of memory. To allow high-speed downloading of waveforms from the system controller (calculator or computer) under DMA control, the ARB Card can transfer characters at a 500-kHz rate. Memory loading has an auto-increment capability so that only the starting waveform address has to be programmed at the beginning of a block waveform load, further optimizing the speed of waveform updates.

Three auxiliary inputs are included on the card to allow use of an external clock, up to 2 MHz, to trigger the waveforms on an external input, and to externally gate or enable the clock. Two auxiliary outputs provide a clock at the programmed sample rate and a synchronization pulse at the end of waveforms in each memory partition.

## CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 53A-241 Card's operating environment.

### Address-Select Switch

The 53A-241 Card has a miniature 10-position switch labeled "ADDRESS" that selects the 53A-241 Card's address (0-9) in the 53/63 Series System. The switch's cover opens to allow the address to be reselected. A screwdriver with a narrow, flat blade should be used to turn the cam-action wiper to the desired address position.

### Power LED

The Power LED provides a valuable diagnostic tool by giving the system programmer a visual indication of the action which the system is currently taking. Whenever the 53A-241 Card is addressed by the system controller, the Power LED goes out. The LED remains out until another function card is addressed. Since only one function card can be addressed at a time, an unlit Power LED indicates the function card with which the system controller is currently communicating. The Power LED being lit not only indicates that the 53A-241 Card is unaddressed, but that all required dc power (5V dc, ±15V dc) is being supplied.

### Fuses

The 5-volt dc and ±15-volt dc power buses each have a fuse that protects the system from overloads. If any fuse has blown, the Power LED will not light.

### Function LEDS and Switches

#### LEDs

The following LEDs are provided at the top front edge of the 53A-241 Card to indicate the status of the card's operation:

RUN A
This LED is lit when partition A of memory is actively transmitting.

RUN B
This LED is lit when partition B of memory is actively transmitting.

PGM A
This LED is lit when partition A of memory is armed for waveform program update.

PGM B
This LED is lit when partition B of memory is armed for waveform program update.

XTRG
This LED is lit when the external trigger has been armed by the X command (see OPERATION section).

## Switches

### External Clock Enable Switch

This SPST switch allows a user-provided, external clock to control the sample rate used by the arbitrary waveform generator. If the switch is in the OFF position, the 53A-241 Card's internal clock is used; if the switch is in the ON position, an external clock can be used by connecting the external clock signal to a designated input pin on the SMB connector (see Appendix B).

## SMB Connector Inputs And Outputs

Six SMB connectors provide the arbitrary waveform output, sample clock output, sync output, external clock input, external trigger input, and external hold input. See Appendix B for a detailed description of these signals.

## SPECIFICATIONS

| | |
|---|---|
| Number of Channels: | Single channel. |
| Resolution: | 10 bits (1024 vertical samples). |
| Memory: | Two 4K memory banks that can be chained to 8K (from 2 to 8,192 horizontal samples). |
| Programming: | ASCII characters representing value of sample in volts. |
| Memory Update Capability: | Random access update of any point in waveforms.<br><br>Automatic increment of address for sequential memory points. |
| Waveform Repeat Capability: | Waveforms A and B are independently programmable for a repeat count of 1 through 99 times, or continuous.<br><br>Repeated waveforms A and B may be chained; chained waveform sequence is programmable for a repeat count of 1 through 99 times, or continuous. |
| Breakpoint Capability: | Any two nonsequential points on waveform can be programmed to pause transmission until card is retriggered. |
| Waveform Triggering: | Triggering under program control, or with external trigger. |
| External Trigger: | Enabled or disabled under program control. |
| Output Amplitude: | ±5 V dc into a 50-Ohm load, ±10 V dc into an open impedance. |
| Output Accuracy | |
| DC Accuracy: | 0.5%. |
| DC Temperature Drift: | 0.02%/°C. |
| Settling Time (Full Scale): | 1.5 μs (to dc accuracy).<br>1.0 μs (to 1.5% accuracy). |
| Output Current: | 100 mA, maximum. |
| Maximum Sample Rate: | 2 MHz. |

| | |
|---|---|
| Programmable Sample Rate: | 2 MHz, 1 MHz, and 400 kHz.<br>200 kHz, 100 kHz, and 40 kHz.<br>20 kHz, 10 kHz, and 4 kHz.<br>2 kHz, 1 kHz, and 400 Hz.<br>200 Hz, 100 Hz, and 40 Hz.<br>20 Hz, 10 Hz, and 4 Hz. |
| External Clock: | User-supplied, 0 to 2 MHz. |
| Frequency Accuracy: | 0.005% (0 °C to 50 °C). |
| Interrupt Capability: | Programmable interrupt at end of transmission, or on breakpoint. |
| Auxiliary I/O Capability: | Sample clock output.<br>End of waveform output.<br>External clock input.<br>External trigger input.<br>Clock enable (gate) input. |
| Auxiliary Outputs: | Advanced Schottky-TTL. |
| Auxiliary Inputs: | One advanced Schottky-TTL load. |
| Power Requirements: | 5V and ±15V dc power is provided by the internal Power Supply in the 53/63 Series Card Cage. |
| Voltage (5-volt Supply): | 4.75 V dc to 5.25 V dc. |
| Current (5-volt Supply): | 1.0 A, maximum quiescent.<br>1.1 A, peak. |
| Voltage: (±15-volt Supplies): | +14.5 V dc to +15.5 V dc.<br>-14.5 V dc to -15.5 V dc. |
| Current (±15-volt Supplies): | 70 mA, maximum quiescent.<br>170 mA, peak. |
| Cooling: | Provided by the fan in the 53/63 Card Cage. |
| Temperature: | -10 °C to +65 °C, operating (assumes ambient temperature of 55 ° and airflow to assure less than 10 °C temperature rise).<br>-40 °C to +85 °C, storage. |
| Humidity: | Less than 95% R.H., noncondensing. |
| Dimensions: | 197 mm high, 221 mm deep, 13 mm wide.<br>(7.75 in x 8.69 in x 0.5 in). |
| Dimensions, Shipping: | When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots. |

When ordered alone, the card's shipping dimensions are:

254 mm x 254 mm x 127 mm.
(10 in x 10 in x 5 in).

Weight: 0.68 kg. (1.5 lb).

Weight, Shipping: When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots.

When ordered alone, the card's shipping weight is:

1.50 kg. (3.3 lbs).

Mounting Position: Any orientation.

Mounting Location: Plugs into a function-card slot of the 53A-002 or 63A-012 Card Cage.

I/O Connections: SMB snap-on connectors; 1 SMB-to-BNC male adapter cable is supplied.

Equipment Supplied:

1 - 53A-241 Arbitrary Waveform Generator Card.
1 - 53A-729 SMB-to-BNC male adapter cable.
1 - Spare fuse (Part # 42202-52003).
1 - Operating manual (Part # 00000-12410).
1 - Service manual (Part # 00000-22410).

# OPERATION

## Overview

The 53A-241 Card is programmed by ASCII characters issued from the system controller to the 53/63 System's communications card. The 53A-241 Card is interfaced to the communications card through the 53 Series or 63 Series Card Cage's backplane.

To address a function card for the first time, the system command @XY must be issued. X is the card cage address (0-9) selected on the 53A-171 Control Card in the addressed card cage; Y is the 53A-241 Card's address (0-9) within the addressed card cage. The 53A-241 Card's address is selected using the card's Address-select switch. Once a function card is addressed, it remains addressed until the system receives another @ character. Appendix A fully discusses the @XY command and the other 53/63 Series System commands. After the 53A-241 Card is addressed, the commands listed below may be issued until another function card is addressed.

## Summary

An overview of the commands in the order they would be typically programmed is as follows:

A or B
: select the A or B partitions of memory, respectively, for voltage programming.

D (Divide) command programs the basic sample rate of the selected portion.

V (Voltage) command sequentially programs the arbitrary waveform voltages for the selected memory partition. It also programs the end-of-waveform bit, any breakpoints, and optional chaining to the waveform in the other partition.

R (Repeat) command programs the number of times to repeat the waveform in the selected memory partition, or programs continuous transmission.

C (Chain) command programs a repeat count or continuous transmission for any chained waveform.

T (Trigger) command starts actual transmission of the waveforms.

H (Halt) command may be used to prematurely halt a waveform or as the means to halt a continuous waveform.

X (eXternal trigger) and I (Interrupt) commands program the external trigger and interrupt modes, respectively.

E (Edit) command allows random access to any location in the selected memory partition for updating of any point or points in the waveform with a subsequent V command.

A status capability for the experienced programmer, to allow synchronization of real-time waveform updates with actual transmission from the two memory partitions, is described in Application Note 241-2.

Card Commands

Detailed descriptions of the 53A-241 Card's commands, in the order listed above, are as follows:

| Command | Description |
|---|---|
| A | The A command selects the A memory partition and resets the memory counters. All commands that follow then set parameters, load, trigger, or edit the A memory partition until the B memory partition is selected. |
| B | The B command selects the B memory partition and resets the memory counters. All commands that follow then set parameters, load, trigger, or edit the B memory partition until the A memory partition is selected.<br><br>*NOTE:* Until instructed to select the other memory partition, the 53A-241 Card always operates on the memory partition currently selected. |

| Command | Description |
|---|---|
| $[n_1n_2]$D | The D (Divide) command specifies how the main sample clock rate is to be divided to form the desired output sample rate as follows: |

"$n_1$" is a 1-digit decimal number (0, 1, or 2) that specifies division of the main sample clock rate (2 MHz) by 1, 2, or 5, respectively.

"$n_2$" is a 1-digit decimal number (0 through 5) that specifies how many times the sample clock rate resulting from the value of "$n_1$" is to be divided by ten. This gives the following possible clock and sample rates:

| Command | Clock Rate | Sample Rate |
|---|---|---|
| 00D | 2 MHz | 500 ns |
| 01D | 200 kHz | 5 µs |
| 02D | 20 kHz | 50 µs |
| 03D | 2 kHz | 500 µs |
| 04D | 200 Hz | 5 ms |
| 05D | 20 Hz | 50 ms |
| 10D | 1 MHz | 1 µs |
| 11D | 100 kHz | 10 µs |
| 12D | 10 kHz | 100 µs |
| 13D | 1 kHz | 1 ms |
| 14D | 100 Hz | 10 ms |
| 15D | 10 Hz | 100 ms |
| 20D | 400 kHz | 2.5 µs |
| 21D | 40 kHz | 25 µs |
| 22D | 4 kHz | 250 µs |
| 23D | 400 Hz | 2.5 ms |
| 24D | 40 Hz | 25 ms |
| 25D | 4 Hz | 250 ms |

On power-up, the value of the D command is undefined. It should be programmed to the desired value after power-up.

The value of the D command is not altered by a Halt command to the card (see H command), or a Halt command or reset to the system (see Appendix A).

| Command | Description |
|---|---|
| [pv][m]V | The V (Voltage) command loads the selected memory partition with:<br><br>1) The desired output voltage to be programmed during a sample period.<br><br>2) The memory programming instructions to be executed during the sample period.<br><br>"pv" is a 1- to 3-digit number, with minus sign and decimal point, which specifies the voltage to be programmed during a sample period. Valid values for "pv" range from -5.11 to 5.11. A plus sign in front of a positive value is optional. The decimal point may be omitted; the card assumes that the 1- to 3-digit number is multiplied by .01. Leading zeros may be omitted, and leading spaces are permitted.<br><br>The programmed voltage value assumes a 50-Ohm load. The unit is calibrated with a 50-Ohm impedance directly on the connector output. For applications where the 50-Ohm load is at the end of a cable, the cable's impedance needs to be taken into consideration in order to achieve the accuracy in the published specifications.<br><br>The output has a 50-Ohm source impedance on the card so that when a very high or open impedance is driven, the output voltage will be twice that programmed, giving a maximum range of -10.22 V to +10.22 V dc.<br><br>For impedances other than 50 Ohms or open, a simple resistance division calculation can be used to calculate the output voltage as follows:<br><br>$V_{out} = 2[pv]R_L / (50.0 + R_L)$<br><br>"m" is a 1-digit decimal number (0 through 7) that specifies the memory programming instructions to be executed, following a T command (see below), during the sample period being programmed. The values of "m" affect executing of the sample period as follows:<br><br>0 Executes the sample at the sample rate.<br><br>1 Chains the memory to the other memory partition (executes the first memory location in the other memory partition next).<br><br>2 End of waveform in memory partition: The sample in the first location in the same memory partition is repeated if the number of times the waveform is to be repeated (programmed with the R command) has not been reached. |

3 Chained end of waveform in memory partition: The waveform programmed in this memory partition is repeated the number of times specified with the R command; then the first location in the other memory partition is executed.

4 Breakpoint: The output holds the current sample until another trigger command is received.

5 Chained breakpoint: The output holds the current sample until another trigger command is received, and then executes the sample in the first location of the other memory partition.

6 Breakpoint and end of waveform: The output holds the current sample until another trigger command is received. The output then executes the sample programmed in the first location of the current memory partition until the waveform is repeated the number of times specified by the R command.

7 Chained breakpoint and end of waveform: The output holds the current sample until another T command is received. When another T command is received, and if the current memory partition has not been repeated the number of times specified by the R command, the next sample executed is the first sample of the current memory partition. When the current memory partition has been repeated the specified number of times, the next sample executed is the first location in the other memory partition.

The values for [pv] and [m] form a single, concatenated number.

Example:

.153V is a valid V command; it programs 0.15 V dc, and sets a chained end of waveform in memory.

Consecutive V commands load into consecutive memory locations. To program a waveform, send an A command or a B command. This resets the memory pointers so that programming begins in the first memory location.

Example of a memory load:

@11A20D00R0.000V1.000V2.000V3.000V4.000V5.002V

The above command is decoded as follows:

The 53A-241 Card is in mainframe 1, card address 1. The A memory partition is being used at a sample rate of 2.5 $\mu$s between samples. The waveform continuously repeats until an H command

or an @XH command is sent. A step function is programmed for 0 V, 1 V, 2 V, 3 V, 4 V, and 5 V, and then repeats.

To start the above command string, send: @11AT

Mainframe 1, card address 1, is again addressed; the memory pointers are reset, and the A memory partition is then triggered.

On power-up, the contents of memory, as programmed by the V command, are undefined. Once programmed, an H command sent to the card, or an @XH command used to reset the 53/63 System (see Appendix A), will not alter the contents of memory as programmed by the V command.

| Command | Description |
|---|---|
| [n]R | The R (Repeat) command specifies the number of times the selected A or B memory partition is to repeat its stored waveform.<br><br>[n] is a 2-digit decimal number, from 00 to 99, that specifies how many times the stored waveform is to repeat. (See the special case using 00R in Example 2).<br><br>Examples:<br><br>1. 99R causes the stored waveform to repeat 99 times.<br><br>2. 00R causes the stored waveform to repeat continuously until the sequence is halted by an @XH command or an H command. |
| [n]C | The C (Chain) command specifies the number of times the chained A and B memory partitions are to repeat.<br><br>[n] is a 2-digit decimal number, from 00 to 99, that specifies how many times the waveform contained in the A and B memories is to repeat. (See the special case using 00C in Example 2).<br><br>Examples:<br><br>1. 46C causes the chained A and B memory sequence to repeat 46 times.<br><br>2. 00C causes the chained A and B memory sequence to repeat continuously until the sequence is halted by an @XH command or an H command. |

| Command | Description |
|---|---|
| X | The X (eXternal trigger) command enables the ARB Card's external-trigger function. After the X command is issued, the ARB Card can be triggered either by sending a T command to the card or by sending an external-trigger pulse to the card's External Trigger Input. The H (Halt) command is used to clear the X command. |
| [n]I | The I (Interrupt) command enables or disables generation of 53/63 System interrupts by the ARB Card.<br><br>[n] is a 1-digit decimal number (0, 1, or 2) that programs the interrupt mode as follows:<br><br>[n] Interrupt Mode<br><br>0 Interrupts disabled.<br><br>1 Breakpoint interrupts enabled. An interrupt is generated whenever a breakpoint occurs, as programmed by the V command with [m] = 4, 5, 6, or 7.<br><br>2 End-of-transmission interrupts enabled. A single interrupt is generated at the completion of the total programmed waveform regardless of whether the waveform is a single-memory-partition waveform, a chained waveform, or a chained or nonchained waveform with a programmed repeat count.<br><br>After an interrupt occurs, it is latched by the ARB Card. The ARB Card will continue to generate the 53/63 System interrupt until the interrupt status of the 53/63 System is checked using the @XS command described in Appendix A. Depending on the type of communications card installed in the 53/63 System, a backplane interrupt will also generate an interrupt back to the system controller. In the case of a 53A-128 Communications Card, for example, a backplane interrupt generates an SRQ (service request) on the IEEE-488 bus. |

| Command | Description |
|---|---|
| T | The T (Trigger) command triggers the ARB Card to being outputting the waveform stored in memory. An A or B command must first be sent to reset the memory pointers to the first sample of the waveform; then the T command is sent. After the T command is sent,the programmed waveform is output at the sample rate specified by the D command, and repeated for the number of times specified by the R command.<br><br>A T command can be issued only when the ARB Card is not currently outputting a waveform. If, for example, the ARB Card is outputting from the A memory and the user wishes to switch to outputting from the B memory, an H command must first be issued to terminate the ARB Card's output before selecting the B memory and issuing another T command. |
| H | The H (Halt) command is used to terminate the ARB Card's output. When the H command is issued, the waveform being output will stop, and the ARB Card's output voltage will go to zero volts.<br><br>Any data previously loaded with the D, V, or I commands will remain unchanged after an H command is issued. If external trigger was selected with the X command, it must be reprogrammed. The repeat count (R command) associated with each memory and the overall chain count (C command) need only be reprogrammed if they were previously programmed for continuous operation. |

| Command | Description |
|---|---|
| [m]E | The E (Edit) command directs a memory location in the waveform sample to be programmed or reprogrammed. The E command is followed by a V command to load the specified memory location. If subsequent V commands are issued, data will be loaded into sequential memory locations following the location specified by the E command.<br><br>The E command may also be issued just prior to a T command to cause the ARB Card's output to begin at a memory location other than 0.<br><br>[m] is a 1- to 4-digit decimal number, from 0 to 4095, that specifies where in memory to begin editing.<br><br>Examples:<br><br>1. 4021E1.120V2.300V directs the value in memory location 4021 of the current memory partition to be changed to 1.12 V, and the value in memory location 4022 to be changed to 2.30 V.<br><br>2. 500ET causes the ARB Card to begin outputting from memory location 500 in the current memory partition. |

## INSTALLATION

The 53A-241 Card is a function card and, therefore, may be plugged into any blue card slot. Setting the address-select switch defines the card's programming address; to avoid confusion, it is recommended that the slot number and the programming address be the same.

**CAUTION:**

To avoid plugging the card in backwards, observe the following:

a. Match the keyed slot on the card to the key in the backplane connector (the component side should be to the right).

b. There are two ejectors on the card. Make sure the ejector marked "53A-241" is at the top.

*NOTE:* The 53A-241 Card requires more +5-volt dc current than the standard 53A function card, limiting the number and placement of 53A-241 Cards in the 53A, the 53B, and the 63A Card Cage installations. Refer to the Power Requirements subsection of the Specifications for more information.

## APPENDIX A

## 53/63 SYSTEM COMMANDS

| Command | Description |
|---|---|
| @XY | The @XY (Address) command addresses a function card in the 53/63 System.<br><br>The @ is a delimiter used by the 53/63 System. The X is a mainframe address (0-9) defined by the address-select switch on the 53A-171 Control Card in the addressed mainframe; the Y is a function card address (0-9) defined by the address-select switch on the function card. Once a mainframe/function-card combination is addressed, it remains addressed until the 53/63 System detects a new @ character. |
| @XS | The @XS (Status) command provides the interrupt status of all function cards within the mainframe defined by X. The mainframe backplane interrupt status of all function cards in the addressed mainframe is latched into the 53A-171 Control Card when the @XS command is issued. All function cards in all mainframes become unaddressed after the @XS command. The 53A-171 Control Card Operating Manual describes the @XS command in detail. The @XS command allows the interrupt status of the 53A-243 Card to be read as programmed by the I (Interrupt) command. |
| @XH | The @XH (Halt) command halts all function cards within the mainframe defined by X. The command does not affect function cards in other mainframes. How a function card reacts to the @XH command depends on the card. The 53A-243 Card reacts as if an H (Halt) command had been issued to the card (see the H command in the OPERATION section) when issued an @XH command. In all cases, an addressed function card (Power LED out) becomes unaddressed (Power LED lit). |
| STOP | The STOP command is not a string of ASCII characters. The command is hard-wired from the system controller (calculator or computer) to the 53/63 System's communications card in each mainframe.<br><br>When the system controller issues a STOP command, each function card, including the 53A-243 Card, reacts as if it received the @XH command described above.<br><br>How the system controller executes the STOP command depends on the communications card used. With the 53A-128 IEEE-488 Card, for example, a STOP command is executed when the system controller asserts the IEEE-488 bus line IFC (Interface Clear) true. |

## APPENDIX B

## INPUT/OUTPUT CONNECTIONS

Snap-on SMB connectors are used for both input and output connections. One 53A-729 SMB-to-BNC Adapter Cable is provided with the card. Additional 53A-729 Adapter Cables may be ordered.

The input/output connectors, from top to bottom, are as follows:

| Pin No. | Signal Name | Function |
|---|---|---|
| J31 | $\overline{\text{EX TRG}}$ | External Trigger Input |
| J41 | $\overline{\text{EX CLK}}$ | External Clock Input |
| J511 | $\overline{\text{EX HOLD}}$ | External Hold Input |
| J512 | $\overline{\text{SYNC}}$ | Sync Output |
| J611 | $\overline{\text{SMPCLK}}$ | Sample Clock Output |
| J612 | ARB OUTPUT | Arbitrary Waveform Output |

External Trigger Input

This input provides external-triggering capability if the input is enabled by the X (eXternal trigger) command (see OPERATION section). The input requires a TTL-compatible, active-low signal. The ARB Card is triggered on the falling edge of the input signal. The minimum pulse width is 120 ns. Actual ARB Card triggering will occur within 1 to120 ns after the falling edge of the external-trigger signal.

External Clock Input

External Clock Input is enabled when the External Clock Enable Switch is set to the ON position (see DESCRIPTION section, Function LEDs and Switches). The input accepts a TTL-compatible signal from 0 Hz to 2 MHz. The clock must be high for a minimum of 45 ns and low for a minimum of 45 ns.

External Hold Input

This input is an asynchronous, TTL, active-low signal; the input disables the sample clock at the next sample output, and holds that output value until the sample time following the removal of the External Hold Input signal. The waveform then continues from the same point where it was when the input went low.

Sync Output

This is a TTL, active-low, output that provides a pulse which is synchronous with the beginning of the analog-output step that completes the waveform programmed by the user. Sync Output repeats each time the program completes the waveform defined by the "end of waveform" argument ([m] = 2, 3, 6, or 7) in the V command (see OPERATION section). The output will remain low for one sample period, and then return high.

Sample Clock Output

This is a TTL, active-low, output that occurs at each sample update. If the internal-clock source is being used, the output will be a square wave whose period is equal to the sample rate programmed by the D command. When an external-clock source is used, the output will be a square wave whose period is equal to the ARB Card's sample rate unless the D command has been programmed to 00D. If 00D is programmed, the output will have a period and duty cycle equal to the supplied external-clock signal.

Arbitrary Waveform Output

This is the analog output of the arbitrary waveform generator. This output can drive a load of 50 Ohms at +5.11 V or a high-impedance load at +10.22 V.

# APPENDIX C

## CALIBRATION PROCEDURE

It is recommended that the 53A-241 Card be calibrated every 12 months in order for the card to meet its published accuracy specifications. Calibration should be carried out in an environment where the temperature is between 21°C and 25°C.

Test Equipment Required:

1. 4 1/2-digit voltmeter with a dc accuracy of ±0.05% of reading.
2. 53A-729 SMB-to-BNC Adapter Cable (supplied with 53A-241 Card).
3. BNC-to-banana plug adapter.

Test Setup:

Using the SMB-to-BNC adapter cable and the BNC-to-banana plug adapter, connect J612 of the 53A-241 Card to the dc-voltage input of the DMM. During the calibration procedure two potentiometers will be adjusted: the offset potentiometer (R811) and the gain potentiometer (R712). The two potentiometers are located at the lower, front edge of the card. The top-most potentiometer is R712; R811 is located directly below R712. See the 53A-241 Card's assembly drawing contained in the 53A-241 Card's service manual for a diagram of the potentiometers' locations.

Calibration Procedure:

1. Send the following command string to the 53A-241 Card:

   @XYHA00R00D0.000V0.002VAT

   where: X = Mainframe address (0-9) selected on 53A-171 Control Card in addressed mainframe

   Y = Card address (0-9) selected on 53A-241 Card's address-select switch

   Adjust the offset potentiometer (R811) so that the DMM reads 0.00 V ± 30 mV.

2. Send the following command string to the 53A-241 Card:

   @XYHA00R00D5.000V5.002VAT

   Adjust the gain potentiometer (R712) so that the DMM reads +10.00 V ±30 mV. Note the exact value of the DMM reading.

3. Send the following command string to the 53A-241 Card:

   @XYHA00R00D-5.000V-5.002VAT

If the DMM reads -10.00 V ±30 mV, proceed to step 4. If the error voltage is not within ±30 mV of -10.00 V, adjust the offset potentiometer (R811) to reduce the error to half of its original value; then proceed to step 4. Note the final error voltage for use in step 4.

Example:

If the DMM reads -9.760 V after issuing the command in step 3, adjust R811 until the DMM reads -9.88 V. The final error voltage is -0.12 V, i.e., -10.00 - (-9.88) = -0.12.

4. Send the following command string to the 53A-241 Card:

@XYHA00R00D5.000V5.002VAT

Calculate the error between the value displayed by the DMM and 10.00 V. If step 3 required no adjustment and the DMM reading is within ±30 mV of 10.00V, proceed to step 9. Otherwise, compare the error voltage computed in this step with the error voltage noted in step 3. The offset potentiometer must then be adjusted to make the error voltages measured in steps 3 and 4 equal. To do this, calculate the sum of the two errors, divide the result by two, and add this quantity to the DMM reading obtained in step 4. Adjust R814 for the desired DMM reading. Note the final error voltage in step 4.

Example:

Using the previous example, the error voltage in step 3 (after the adjustment of R811 was -0.12 V. If the initial voltage measured in step 4 was 9.98 V, the error voltage in step 4 is 0.02 V. (-0.12 + 0.02)/2 = -0.05. R811 is then adjusted so that the DMM reads 9.93 (9.98 - 0.05). The final error voltage in step 4 is 0.07 V.

5. Send the following command string to the 53A-241 Card:

@XYHA00R00D-5.000V-5.002VAT

Calculate the magnitude of the error between the value displayed by the DMM and -10.00 V. If this value has the same magnitude as the final error voltage in step 4, proceed to step 6. Otherwise, use the procedure in step 4 (using the magnitude of error calculated in step 5 rather than the step 3 value) to again adjust the offset potentiometer. Repeat steps 4 and 5 until the magnitudes of the errors at +10.00 V and -10.00V are the same.

6. Send the following command string to the 53A-241 Card:

@XYHA00R00D5.000V5.002VAT

Adjust the gain potentiometer (R712) until the value displayed on the DMM is +10.00 V ±30 mV.

7. Send the following command string to the 53A-241 Card:

@XYHA00R00D-5.000V-5.002VAT

Adjust the gain potentiometer (R712) until the value displayed on the DMM is 10.00 V ±30 mV.

8. Repeat steps 6 and 7 until no further adjustment is necessary.

9. Send the following command string to the 53A-241 Card:

   @XYHA00R00D0.000V0.002VAT

   If the DMM reading is 0.00 V +30 mV, proceed to step 12. If the DMM reading is greater than ±30 mV, adjust the offset potentiometer (R811) until the DMM reads 0.00 V ± 30 mV.

10. Send the following command string to the 53A-241 Card:

    @XYHA00R00D5.000V5.002VAT

    If the DMM reading is within ±30 mV of 10.00 V, proceed to step 11. If it is not, adjust the gain potentiometer (R712) so that the DMM reading is 10.00 V ±30 mV.

11. Send the following command string to the 53A-241 Card:

    @XYHA00R00D-5.000V-5.002VAT

    If the DMM reading is within ±30 mV of -10.00 V, proceed to step 12. Otherwise, adjust the gain potentiometer (R712) so that the DMM reading is -10.00 V ±30 mV.

12. This step is a final linearity check of the 53A-241 Card. Send each of the commands listed below, and then check that the DMM reading is within ±30 mV of the listed desired voltmeter reading. If any measurement is out of tolerance, adjust the offset potentiometer (R811) by the minimum amount needed to bring the measurement into tolerance. If any adjustments are made, the sequence from step 8 through step 12 must be repeated.

| Commands to be Sent | Desired Voltmeter Readings (V) |
|---|---|
| @XYHA00R00D-5.120V-5.122VAT | -10.24 |
| @XYHA00R00D-5.110V-5.112VAT | -10.22 |
| @XYHA00R00D-5.100V-5.102VAT | -10.20 |
| @XYHA00R00D-5.080V-5.082VAT | -10.16 |
| @XYHA00R00D-5.040V-5.042VAT | -10.08 |
| @XYHA00R00D-4.960V-4.962VAT | -9.92 |
| @XYHA00R00D-4.800V-4.802VAT | -9.60 |
| @XYHA00R00D-4.480V-4.482VAT | -8.96 |
| @XYHA00R00D-3.840V-3.842VAT | -7.68 |
| @XYHA00R00D-2.560V-2.562VAT | -5.12 |
| @XYHA00R00D0.000V0.002VAT | 0.00 |
| @XYHA00R00D0.010V0.012VAT | 0.02 |
| @XYHA00R00D0.020V0.022VAT | 0.04 |
| @XYHA00R00D0.040V0.042VAT | 0.08 |
| @XYHA00R00D0.080V0.082VAT | 0.16 |
| @XYHA00R00D0.160B0.162VAT | 0.32 |
| @XYHA00R00D0.320V0.322VAT | 0.64 |
| @YYHA00R00D0.640V0.642VAT | 1.28 |
| @XYHA00R00D1.280V1.282VAT | 2.56 |
| @XYHA00R00D2.560V2.562VAT | 5.12 |
| @XYHA00R00D5.110V5.112VAT | 10.22 |

# APPENDIX D

## APPLICATION NOTE 241-1

### Synthesis of Sinusoidal Waveforms

This application note describes an algorithm for programming the 53A-241 Arbitrary Waveform Generator Card as a sine-wave synthesizer. Input parameters to the algorithm are the sine wave's frequency, peak-to-peak amplitude, dc off-set, and the number of points to be programmed in the 53A-241 Card's memory. A sample BASIC program is provided at the end of this application note to implement the algorithm.

The 53A-241 Card can be programmed for 18 different sampling frequencies while using as many as 8,192 points in the ARB Card's memory. Depending on the value of the desired waveform frequency, the sampling frequency and number of data points used can be adjusted to produce the exact (or almost exact) waveform frequency desired. If the desired frequency cannot be programmed exactly, a minimum error between the desired frequency and the actual frequency programmed can be achieved by using the maximum number of points possible in memory and an intelligently chosen sampling frequency.

The closest possible frequency (or if the frequency is exact, the waveform with the least distortion) can be achieved by selecting a sampling frequency from Table 241-1. However, as the number of sample points increases, the time required to compute the points and load them into the ARB Card's memory often becomes objectionable; and a waveform with fewer sample points must therefore be chosen. The example shown is for a 312.5-Hz sine wave. Distortion is expressed as the maximum level of harmonic and other spurious noise (in dB) below the 312.5-Hz signal, occurring in a bandwidth of dc to 250 kHz.

A typical compromise between waveform accuracy, distortion, and sample- computation time, is to use a waveform constructed with 100 to 300 sample points. The sample BASIC program presented at the end of this application note uses from 120 to 300 points to construct waveforms from 5 Hz to 80 kHz with a resulting maximum frequency error of ±0.41% and a distortion of < -40 dB.

The waveform frequency will be the sampling frequency divided by the number of points in the waveform.

#### Waveform Distortion

| Number of Sample Points | Distortion (dB) | THD (%) |
|---|---|---|
| 6400 | < -35.0 | 0.03 |
| 640 | < -25.0 | 0.3 |
| 160 | < -19.0 | 1.3 |
| 120 | < -17.8 | 1.6 |
| 64 | < -15.0 | 3.2 |

Once a sample rate has been chosen, the algorithm for generating the voltage values for the points in memory is as follows:

$$V_i = V_{dc} + 1/2V_{ptp} \sin[6.283185 \cdot i \cdot (F_o/F_s)]$$

where:

| | | |
|---|---|---|
| $V_i$ | = | voltage of ith point in ARB Card's memory, i = 1 to n |
| $V_{dc}$ | = | dc offset voltage |
| $V_{ptp}$ | = | peak-to-peak voltage |
| $F_o$ | = | programmed output frequency |
| $F_s$ | = | sampling frequency of ARB Card |

The number of points to be programmed is determined by dividing the ARB Card's sampling frequency (D command) by the desired frequency.

Sample Program

The sample program shown below is written in Advanced BASIC (BASICA) for an IBM PC. The PC is connected to the CDS card cage using a 53A-903 I/O Card installed in the PC. The 53A-903 I/O Card provides an IEEE-488 interface between the PC and the CDS card cage. The 53A-241 Card has been set to address 9. The address of the 53/63 System's card cage containing the 53A-241 Card is address 1.

The sample program loads the memory of the 53A-241 Card using the preceding algorithm, and triggers the card to output the waveform. The waveform frequency, peak-to-peak voltage, and dc offset are input when the program is run. The 5-Hz to 80-kHz sine wave developed will have a maximum frequency error of ±0.41%, and exhibit a distortion of < -40 dB.

Lines 1090 through 1130 define the waveform's frequency and voltage parameters. Lines 1140 through 1460 develop the waveform's voltage points to load into the ARB Card's memory. The CALL statements at lines 1480, 1510, and 1540 transfer the contents of the string variable WRT$ to the 53A-241 Card.

In the program listing, lines which are not preceded by a line number are not part of the BASIC program. They are inserted as comments to explain what is occurring at each numbered line.

.
.
.

```
1090 INPUT "ENTER SINE WAVE'S FREQUENCY IN HERTZ ",FO
1100 INPUT "ENTER SINE WAVE'S PTP VOLTAGE IN VOLTS ",VPP
1110 INPUT "ENTER SINE WAVE'S DC OFFSET IN VOLTS ",VDC
```

Define variables for the output waveform's frequency (FO), peak-to-peak voltage (VPP), and dc offset voltage (VDC).

```
1120 IF FO > 80000 THEN PRINT "FREQUENCY OUT OF LIMITS": GOTO 1550
1130 IF (VDC + 0.5*VPP) > 5.11 OR (VDC - 0.5*VPP) < -5.11 THEN PRINT "OUT-OF-LIMIT
     VOLTAGE ATTEMPTED": GOTO 1550
```

Determine if the maximum frequency or output level has been exceeded.

*NOTE:* The output voltage will equal the programmed voltage only when the ARB Card is driving a 50-Ohm load. See the V command in the OPERATION Section.

```
1140 PTS = FO*120
1150 IF PTS <= 2E6 AND PTS > 1E6 THEN SR$ = "00D": N=2E6/FO: GOTO 1330
1160 IF PTS <= 1E6 AND PTS > 4E5 THEN SR$ = "10D": N=1E6/FO: GOTO 1330
1170 IF PTS <= 4E5 AND PTS > 2E5 THEN SR$ = "20D": N=4E5/FO: GOTO 1330
1180 IF PTS <= 2E5 AND PTS > 1E5 THEN SR$ = "01D": N=2E5/FO: GOTO 1330
1190 IF PTS <= 1E5 AND PTS > 4E4 THEN SR$ = "11D": N=1E5/FO: GOTO 1330
1200 IF PTS <= 4E4 AND PTS > 2E4 THEN SR$ = "21D": N=4E4/FO: GOTO 1330
1210 IF PTS <= 2E4 AND PTS > 1E4 THEN SR$ = "02D": N=2E4/FO: GOTO 1330
1220 IF PTS <= 1E4 AND PTS > 4E3 THEN SR$ = "12D": N=1E4/FO: GOTO 1330
1230 IF PTS <= 4E3 AND PTS > 2E3 THEN SR$ = "22D": N=4E3/FO: GOTO 1330
1240 IF PTS <= 2E3 AND PTS > 1E3 THEN SR$ = "03D": N=2E3/FO: GOTO 1330
1250 IF PTS <= 1E3 AND PTS > 4E2 THEN SR$ = "13D": N=1E3/FO: GOTO 1330
1260 IF PTS <= 4E2 AND PTS > 2E2 THEN SR$ = "23D": N=4E2/FO: GOTO 1330
1270 IF PTS <= 2E2 AND PTS > 1E2 THEN SR$ = "04D": N=2E2/FO: GOTO 1330
1280 IF PTS <= 1E2 AND PTS > 4E1 THEN SR$ = "14D": N=1E2/FO: GOTO 1330
1290 IF PTS <= 4E1 AND PTS > 2E1 THEN SR$ = "24D": N=4E1/FO: GOTO 1330
1300 IF PTS <= 2E1 AND PTS > 1E1 THEN SR$ = "05D": N=2E1/FO: GOTO1330
1310 IF PTS <= 1E1 AND PTS > 4E0 THEN SR$ = "15D": N=1E1/FO: GOTO 1330
1320 SR$ = "25D": N = 4/FO
1330 J = 1: K = 0
1340 LET N = CINT(N)
```

The value 120 in line 1140 determines the minimum number of voltage points a waveform will contain. Lines 1150 through 1320 determine the exact number of voltage points and the ARB Card's sampling frequency. N is the number of points to be programmed. The CINT function in line 1340 rounds N to the nearest integer, providing the closest frequency to the desired frequency. The string variable SR$ contains the required command string to program the ARB Card's sampling frequency.

```
1350 C$ = "@19HA00R" + SR$
```

C$ is a string used to define setup commands for the 53A-241 Card.

@19 is the @XY (Address) command.
H is the Halt command.
A selects the A memory partition.
00R programs the waveform to repeat continuously.
SR$ contains the D command for the ARB Card's sampling frequency.

```
1360 LET C1 = (6.283185)/N
1370 LET C2 = .5*VPP
```

C1 and C2 are constants used in computing the ARB Card's output-voltage steps. C1 is in radians because the SIN function in line 1390 requires radians rather than degrees.

```
1380 FOR I = 1 TO N
1390 V = VDC + C2*SIN(C1*I)
1400 V% = CINT(V*100)
1410 V$ = STR$(V%)
1420 IF I < N THEN V$ = V$ + "0V": GOTO 1440
1430 IF I = N THEN V$ = V$ + "2V"
```

Compute the Ith output-voltage step, convert the result to an integer, convert the integer to a character string, and append the memory-programming instruction code and an ASCII V.

```
1440 D$(J) = D$(J) + V$: K = K + 1
1450 IF K = 36 THEN K = 0: J = J + 1
1460 NEXT I
```

Append the Ith data point to the D$-array element D$(J). When a D$-array element contains 36 voltage steps, increment the D$-array subscript J. When the FOR-NEXT loop from 1 to N is complete, the D$ array will contain the voltage points to be loaded into the ARB Card's memory.

```
1470 WRT$ = C$
1480 CALL IBWRT(CDS%,WRT$)
1490 FOR I = 1 TO J
```

Output the setup commands to the ARB Card

```
1500 WRT$ = D$(I)
1510 CALL IBWRT(CDS%,WRT$)
1520 NEXT I
```

Output the voltage points to the ARB Card.

```
1530 WRT$ = "AT"
1540 CALL IBWRT(CDS%,WRT$)
1550 END
```

Reset the A memory pointer to the beginning of memory, and trigger the card.

## APPENDIX E

## APPLICATION NOTE 241-2

### Considerations for "On-the-Fly" Updating of the ARB Card's Memory

When the two memory partitions of a 53A-241 Card are chained together, it is often desirable to update one memory partition while the other partition is being output. This application note describes and discusses the factors that must be considered to determine if a given 53A-241 Card/system-controller configuration is suitable for doing "on-the-fly" updating of a memory partition.

Four factors must be considered before using the ARB Card's "on-the-fly" updating capability:

1. The total amount of time it will take the system controller to output the new data to the memory partition.

2. The total time required by the 53/63 System and the ARB Card to accept and process the new output data.

3. The total time available for updating the ARB Card's memory partition.

4. The total time required for the system controller to obtain the status of the ARB Card and branch to the memory-update routine.

For successful "on-the-fly" updating, the above considerations can be reduced to the following inequality:

$$T_A > T_S + T_P + T_{STAT}$$

where:

$T_A$ = Total time available for updating a memory partition

$T_S$ = Total time required by system controller to output new data

$T_P$ = Total time required for the ARB Card and 53/63 System to process the new data

$T_{STAT}$ = Total time required for the system controller to obtain the status of the ARB Card and branch to the memory-update routine

To define $T_S$, consult the documentation provided by the system controller's manufacturer to determine the system controller's output rate. When determining the system controller's output rate, be aware that controller manufacturers typically specify the output rate for the 2nd to nth output-data bytes. The output time for the first output byte is generally much greater. High- performance system controllers typically provide a 0.3-ms to 2.0-ms transfer time for the first output byte and a 3-us to 5-us transfer time for the 2nd to nth output bytes when multiple bytes are output by a single output statement from the system controller.

Six bytes of data (e.g., -5231V) are normally output to update a single data point. The total time to output K data points, with a single output statement from the system controller, is as follows:

$$T_S = T_{S1} + T_{S2}(6K - 1)$$

where: $T_S$ = Total output time for K data points

$T_{S1}$ = Time for system controller to output first byte

$T_{S2}$ = Time for system controller to output each of the 2nd through nth bytes

K = Number of data points being output

The time required for the 53/63 System and the ARB Card to accept and process each new data point is a function of the communications card installed in the 53/63 System. In the case of a 53A-128 IEEE-488 Communications Card, for example, 7.5 µs are required for the communications card to process a single data byte, and 2.0 µs are required for the ARB Card to process the same data byte. If K data points (six bytes per point) are to be updated in the ARB Card's memory, then the total time needed for the 53/63 System and the ARB Card to process the resulting data transfer is as follows:

$$T_P = 9.5\ \mu s \times 6 \times K$$

where: $T_P$ = Total time needed to process K data points

The total time available for updating a memory partition is a function of the number of data points and the sample rate programmed for the memory partition currently being output (i.e., partition B will be updated while partition A is being output). This time is defined as follows:

$$T_A = J \times D$$

where: $T_A$ = Total time available for updating a memory partition

J = Number of data points in the memory partition currently being output

D = Sample rate programmed with D command

$T_{STAT}$ is the time required for the system controller to obtain the status of the ARB Card, determine that the card has switched from one memory partition to the other, and then branch to the memory-update routine. Updating of the ARB Card's memory should begin immediately after the card switches outputting from one memory partition to the other memory partition.

The memory partition currently being output by the ARB Card can be determined at any time by addressing the card (@XY command) and requesting input from the card. A single byte of data will be returned. This byte will not be followed by <CR><LF> characters. If the A partition is currently being output, the byte will be a binary 0 (hex 00). If the B partition is being output by the card, the byte will be a binary 1 (hex 01).

$T_{STAT}$ is defined as follows:

$$T_{STAT} = T_I + T_C + 9.5\ \mu s$$

where: $T_{STAT}$ = Time required to obtain status

$T_I$ = Time required for system controller to input one data byte

$T_C$ = Time required for system controller to determine if ARB Card has switched memory partitions and, if so,branch to the memory-update routine

The 9.5 µs in the above equation is the time required for the ARB Card to output the memory partition's status byte when a 53A-128 IEEE-488 Communications Card is being used in the 53/63 System. To determine $T_I$ and $T_C$, consult the documentation provided by the system controller's manufacturer. When determining $T_I$ be sure that the time used is the time required to input the first byte, not the 2nd through nth bytes. High-performance system controllers typically require 0.3 to 2.0 ms to input a single data byte. Determining TC will require "blocking out" the system controller's code for detecting when the ARB Card switches memory partitions, and then branching to the memory-update routine. You will need to determine the system controller's execution time for each instruction used.

To successfully update one memory partition while another is being output, the following inequality must be satisfied:

$$T_A > T_S + T_P + T_{STAT} + T_{SF}$$

where: $T_{SF}$ = Safety factor (approximately 15% of $T_S + T_P + T_{STAT}$)

$T_S$, $T_P$, and $T_{STAT}$ are as defined above.

$T_{SF}$ is included to allow for inaccuracies in computing the various timing considerations. If the ARB Card should switch from partition A to partition B while B is still being updated, incorrect ARB Card operation will occur.

In summary, to determine if one memory partition can be updated "on-the-fly" while the other memory partition is being output, a detailed analysis must be made of the system controller's input/output data rates, the 53/63 System's and ARB Card's byte-by-byte processing time, and total available update time.